Sequential Logic

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Overview
Part 1

- K-Maps with Don’t Care midterms
- Combinational and Sequential Logic
- Inputs, Outputs and States
- Set Latch
- Reset Latch
- SR Latch
    - Feedback with NOR gates
    - Timing Diagram
    - Truth Table and K-Map
    - Feedback with NAND gates
- Gated SR and Gated Delay Latches
    - Wrapper on SR Latch
    - Truth Table and K-Map
    - Feedback Logic

Overview
Part 2

- Master-Slave SR Flip Flop
  - Circuit
  - Timing Diagram
- Master-Slave D Flip Flop
  - Circuit
  - Timing Diagram
- Edge-Triggered Flip Flop
  - Propagation Delay
  - Setup/Hold Time

Overview
Part 3

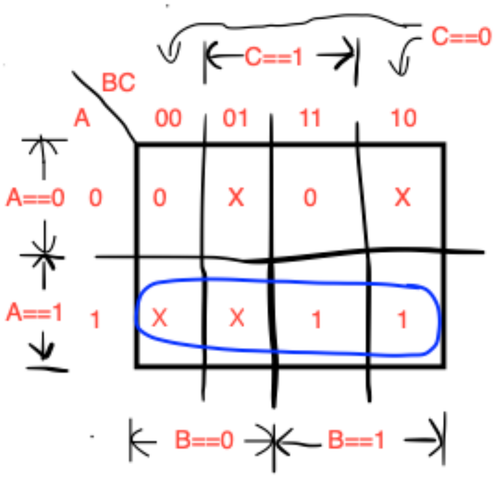
- Counter
- Moore/Mealy State Machine Design
- Register File
- Memory

K-Maps

Don’t Care minterms

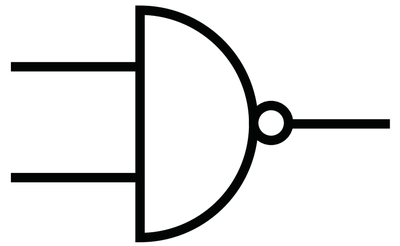
- Some minterm outputs could be 0 or 1
  - Customer doesn’t care
- Example:
  - A: 1 if temperature is greater than 80 degrees
  - B: 1 if temperature is greater than 70 degrees
  - C: 1 if sunny
  - Z=1 when Air Conditioning should be on
    - If T > 80, Turn on
    - If not sunny and 70 < T < 80, Don’t care
    - If sunny and temp. < 70 degrees, Don’t care

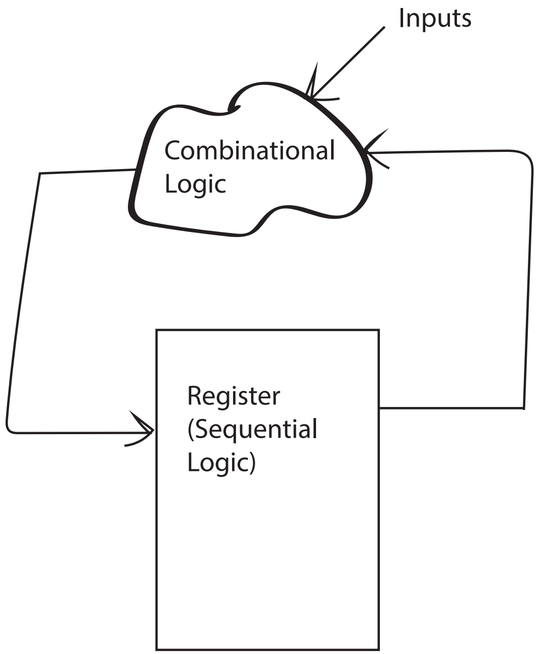
A	B	C	Q
0	0	0	0
0	0	1	X (Don’t Care)
0	1	0	X (Don’t Care)
0	1	1	0
1	0	0	X (Invalid)
1	0	1	X (Invalid)
1	1	0	1
1	1	1	1



Combinational and Sequential Logic

- Combinational Logic
  - Logic gates (AND, OR, NOT, NAND, etc.)
  - Output depends only on input(s)
- Sequential Logic
  - Output depends on input(s) and/or current state of system
  - Store state
  - Retain value as long as power is present
    - Will look at memory in next lecture



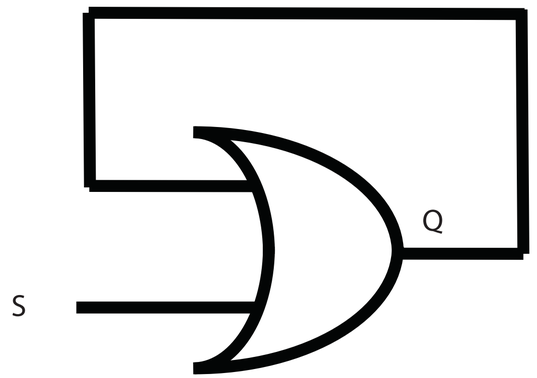


Inputs, Outputs and States

- Inputs:
  - Thermometer reading (outside car): degrees Fahrenheit rounded to integer
  - Weather: Sunny (0), Cloudy (1), Windy (2), Rainy (3), Snowy (4), etc.
  - Desired inside temperature: degrees Fahrenheit rounded to integer
  - Thermometer reading (inside car): degrees Fahrenheit rounded to integer
  - Mode: Auto (0), A/C off (1), A/C on (2)
- State:
  - Current A/C level: 0-3
- Output:
  - Change A/C level: No change (0), Increase (1), Decrease (2)
    - Internal: changes value of “Current A/C level” state
  - LED screen: show current A/C level

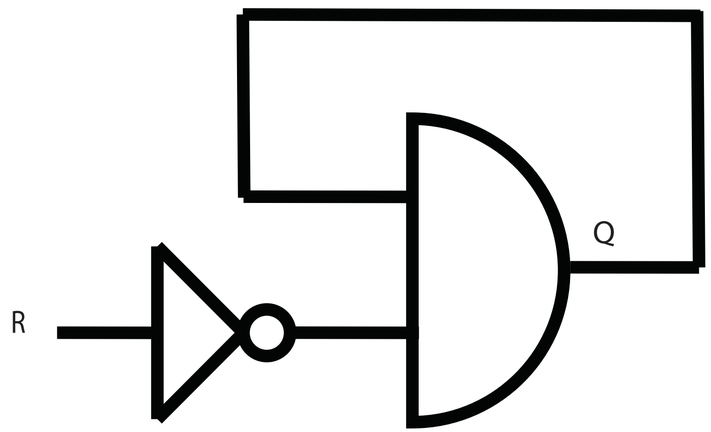
Set Latch

- S input == 1: force output to 1
  - OR gate input
- S input == 0: preserve output value
  - OR gate's 2nd input



Reset Latch

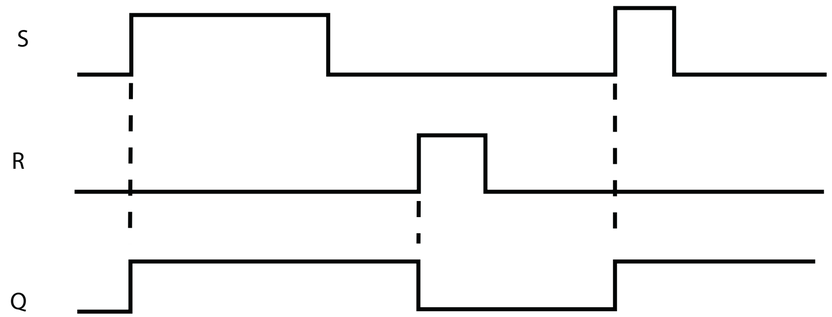
- R input == 1: force output to 0
  - R’: AND gate’s input
- R input == 0: preserve output value
  - Q: AND gate’s 2nd input



SR Latch

Requirements and Timing Diagram

- S input == 1: force output to 1
- R input == 1: force output to 0
- S and R inputs == 0: preserve output
- S and R inputs == 1:
  - Output cannot be both 1 and 0
  - Invalid entry
    - Don’t care: Design can pick S or R

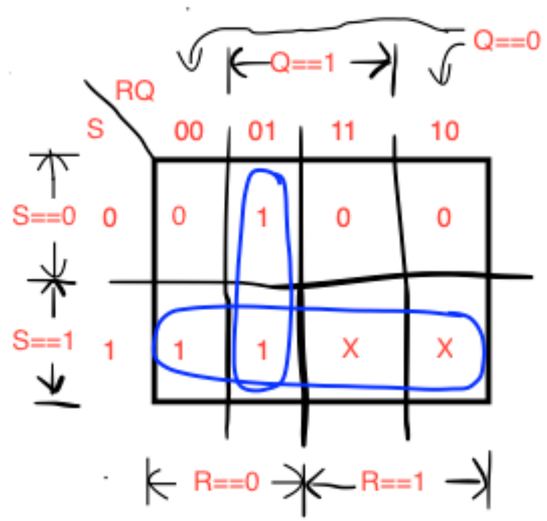


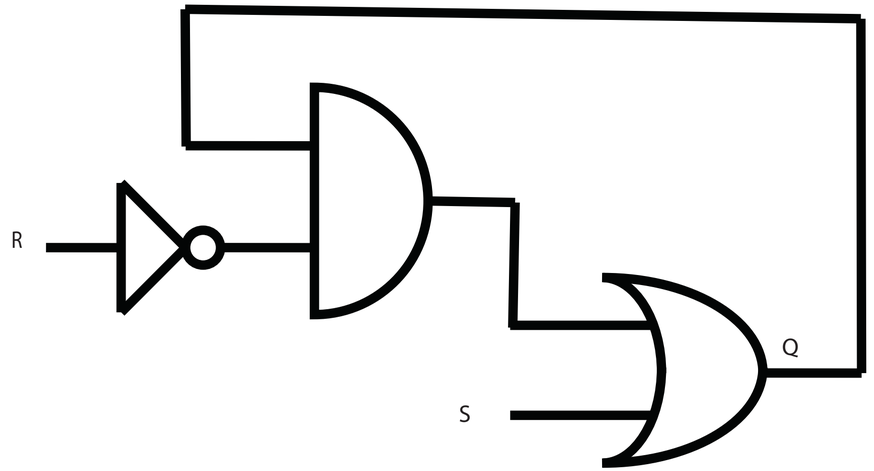
SR Latch

Truth Table & K-Map

- $Q_{new} = S + R'Q_{old}$

S	R	Q (Old)	Q (New)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

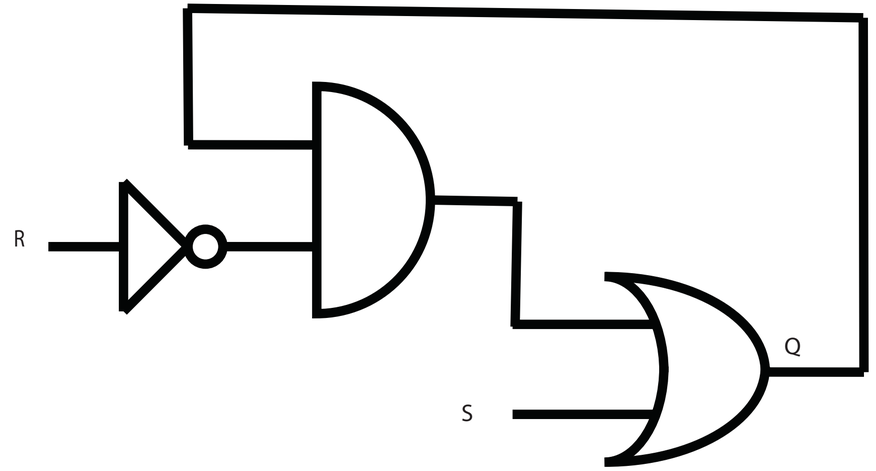


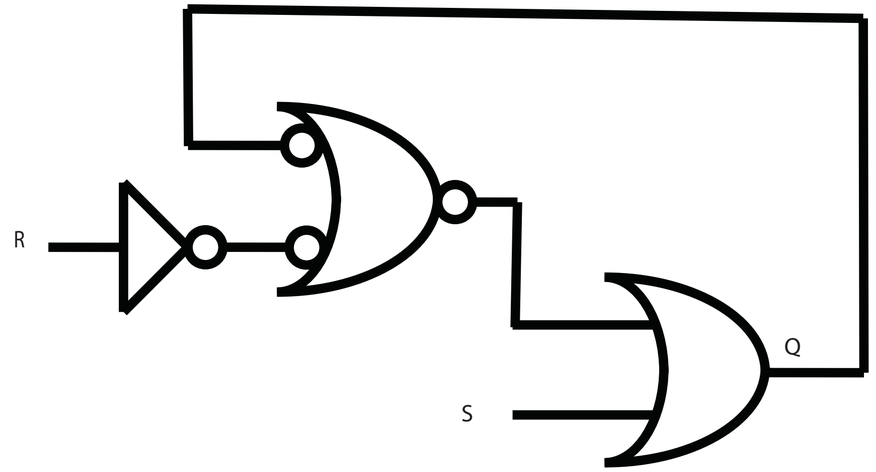


SR Latch

Design

- S input == 1: force output to 1
- R input == 1: force output to 0
- S and R inputs == 0: preserve output
- Use combination of S latch and R latch
- Re-arrange to use NOR gates
  - AB = (A’ + B’)’





SR Latch

Design

- S input == 1: force output to 1
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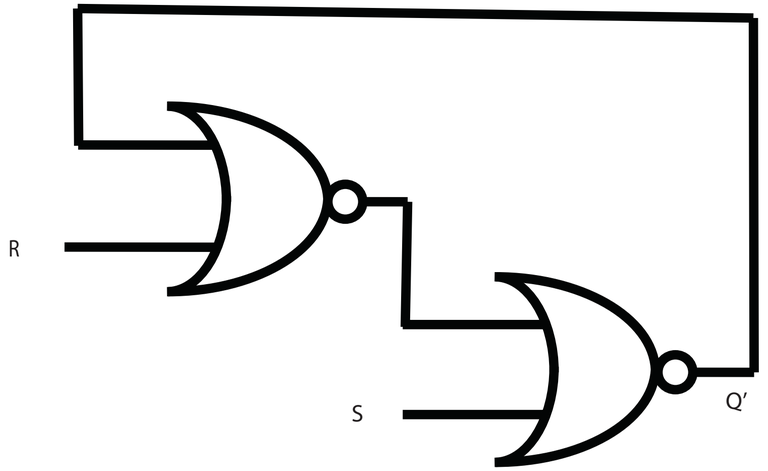
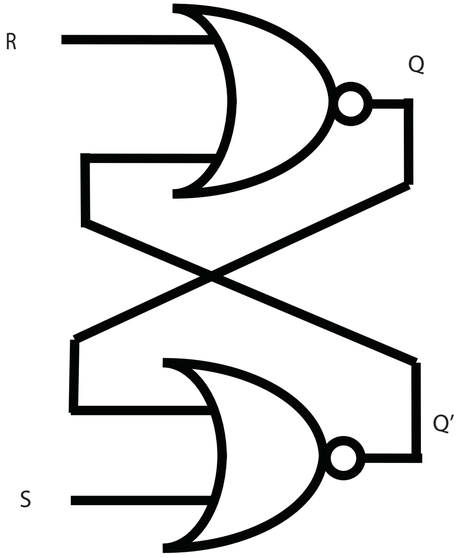
- S and R inputs == 0: preserve output
- Use combination of S latch and R latch
- Re-arrange to use NOR gates
  - AB = (A’ + B’)’
  - A + B = (A’B’)’

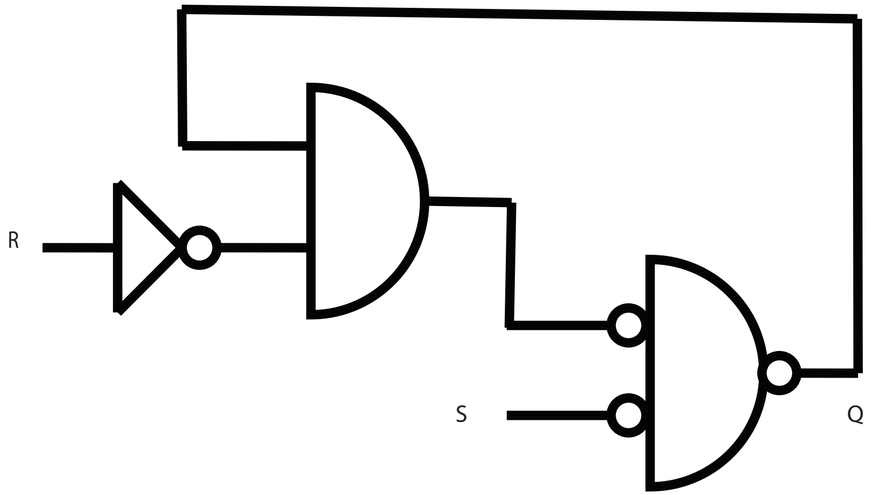


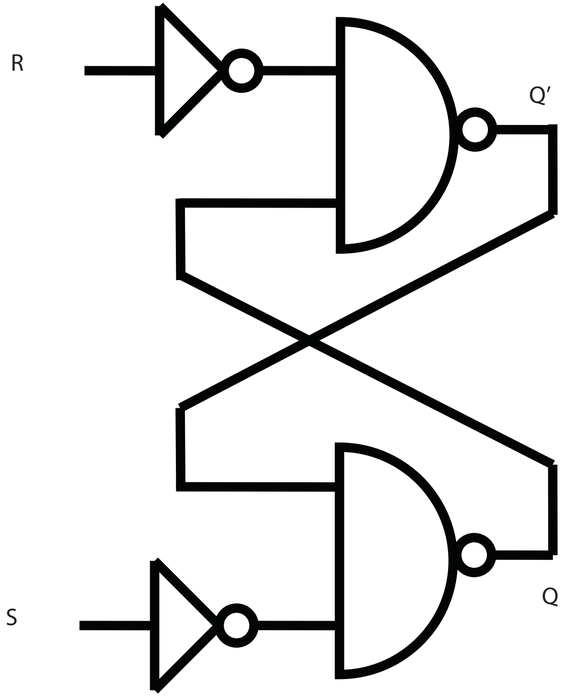


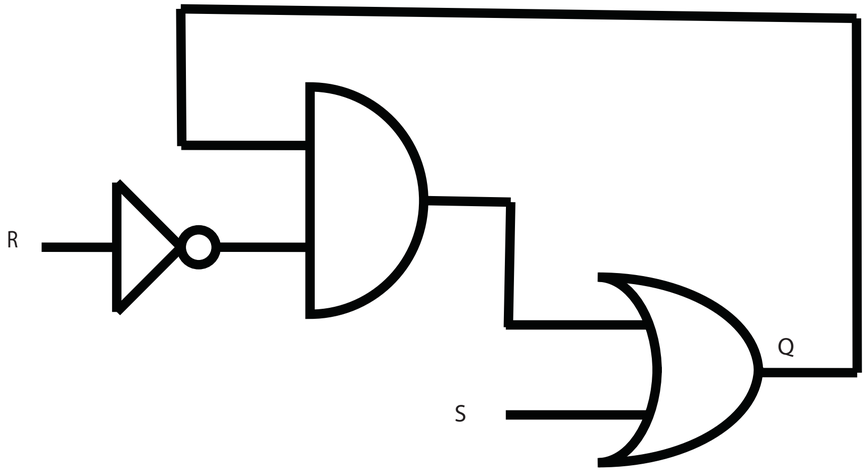
SR Latch

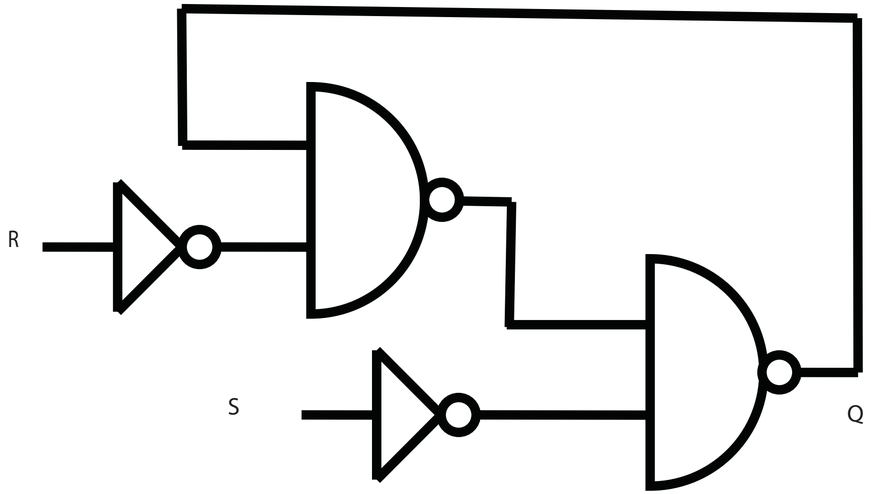
NAND Gates

- $Q_{new} = S + R'Q_{old}$
- $A + B = (A'B')'$





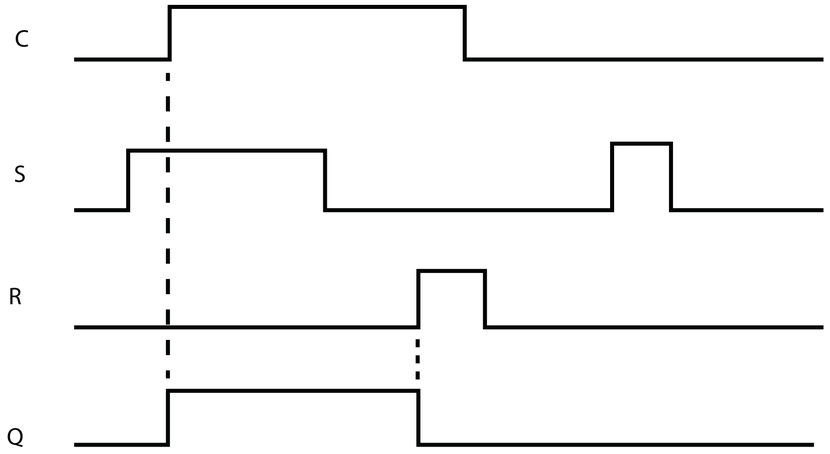




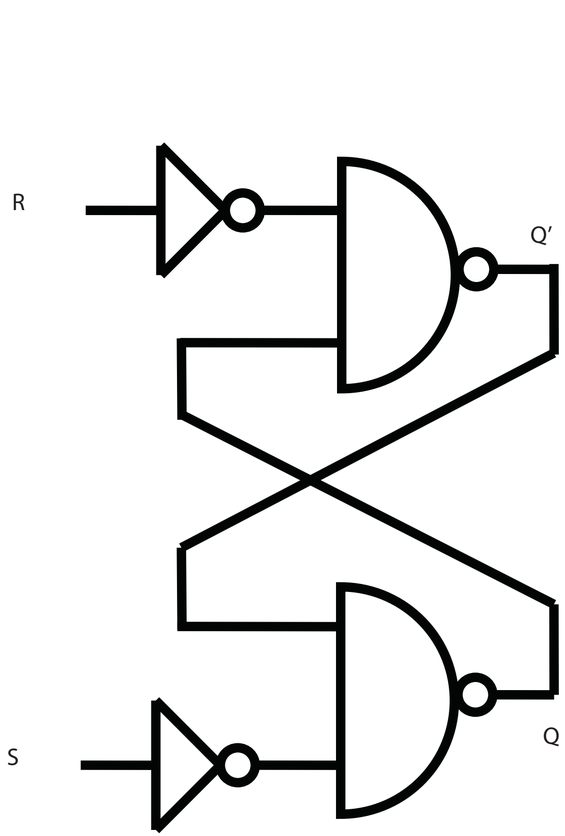
Gated SR Latch

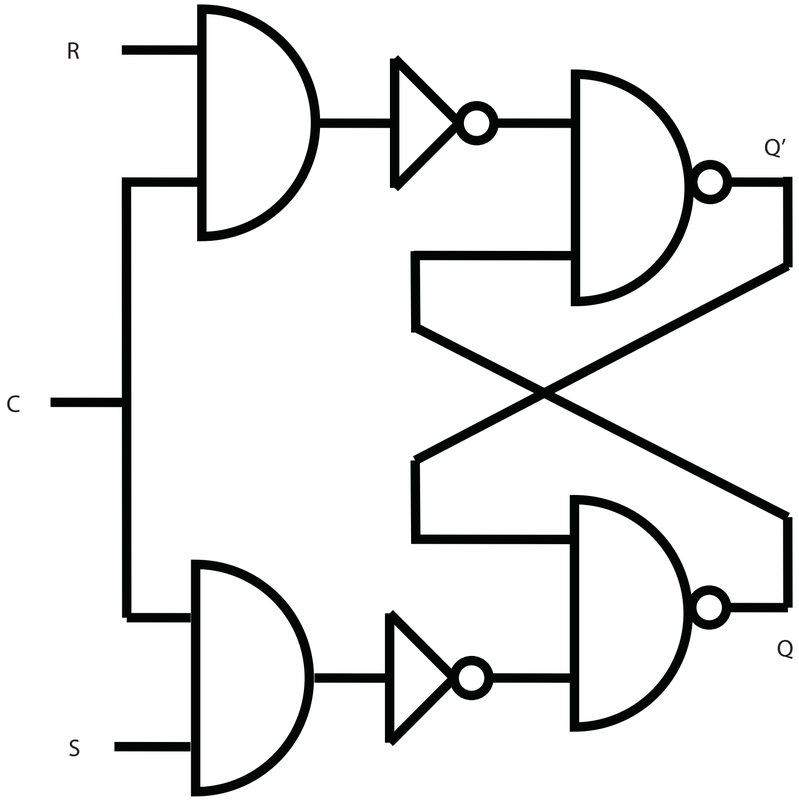
Requirements and Timing Diagram

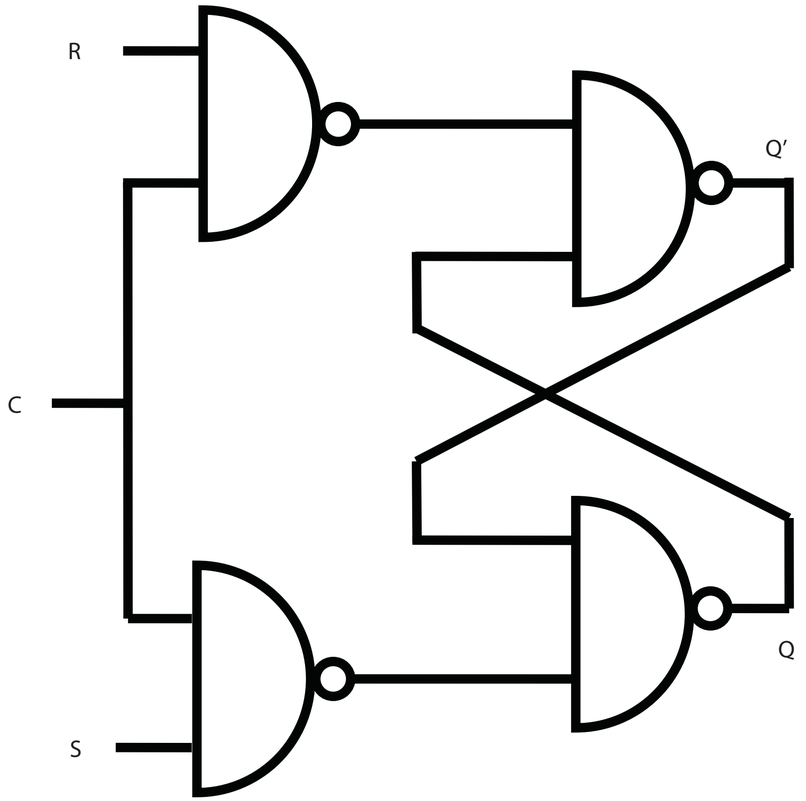
- **C input == 0: Don’t allow any change to Q**
- **C input == 1: Allow Set/Reset**
- S input == 1: force output to 1
- R input == 1: force output to 0
- S and R inputs == 0: preserve output
- S and R inputs == 1:
  - Output cannot be both 1 and 0
  - Invalid entry
    - Don’t care: Design can pick S or R



Gated SR Latch



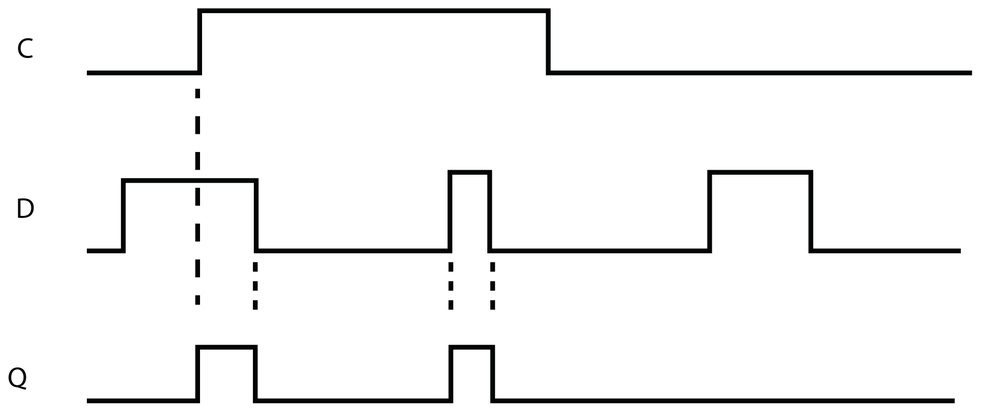




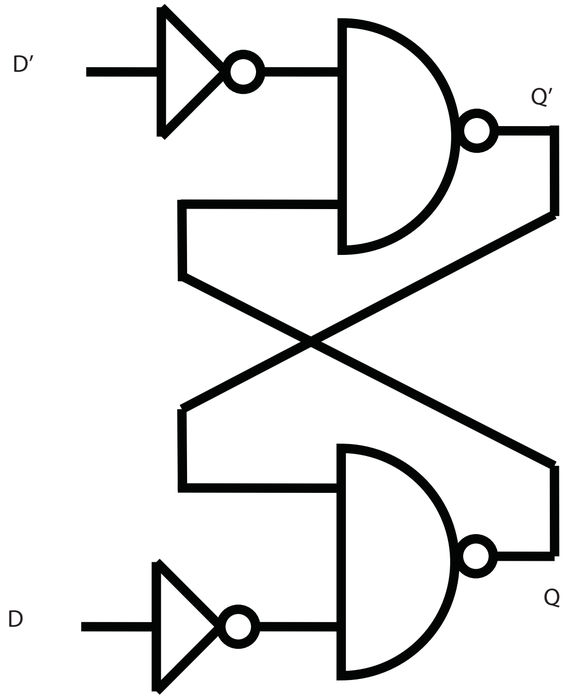
Gated D Latch

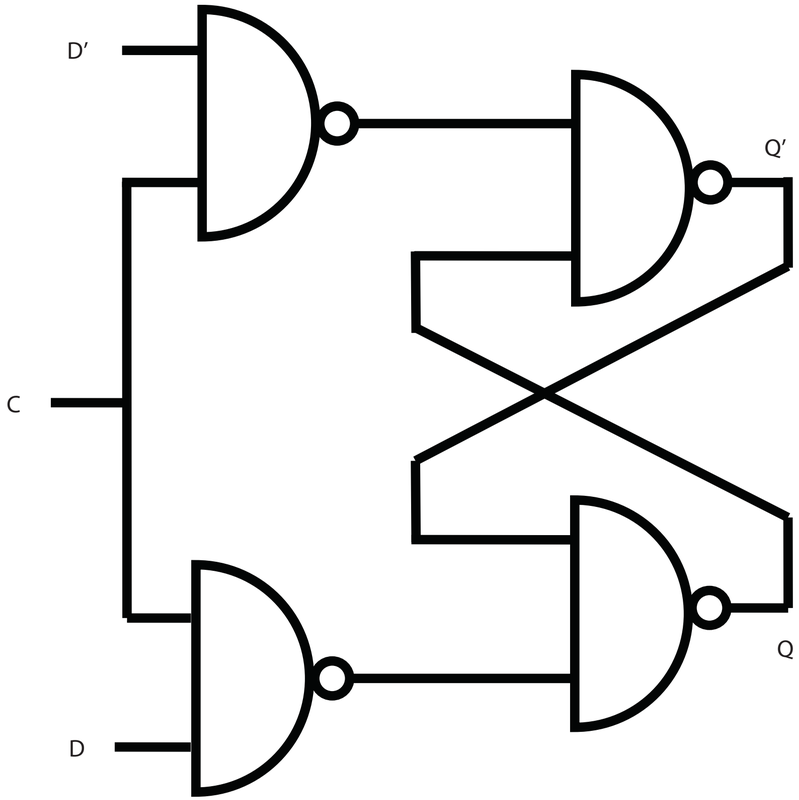
Requirements and Timing Diagram

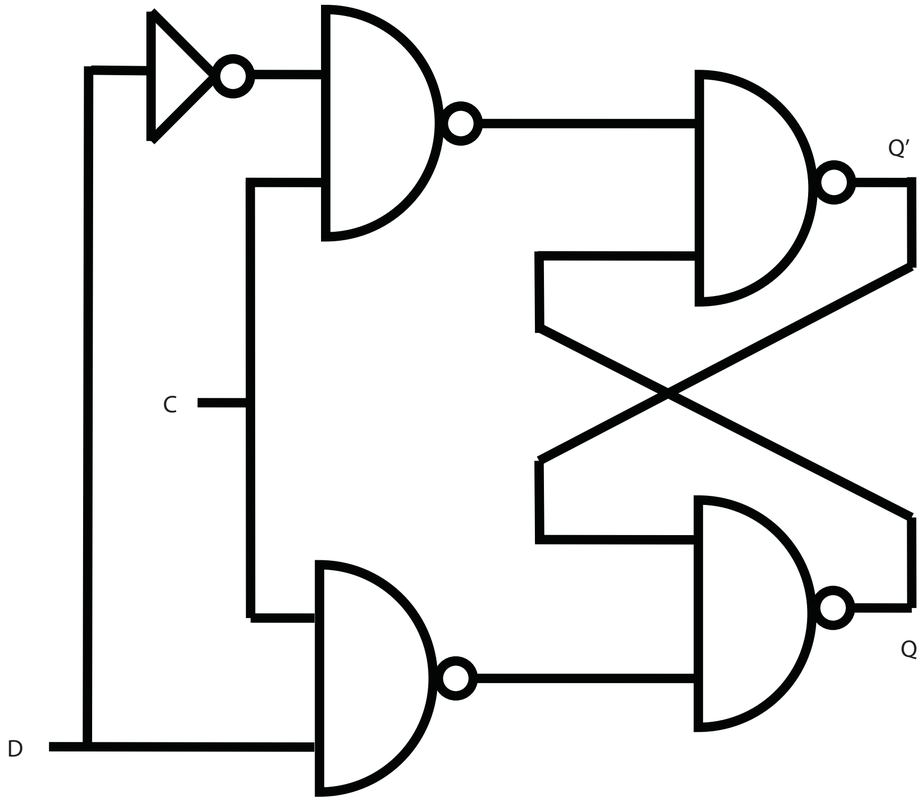
- **C input == 0: Don’t allow any change to Q**
- **C input == 1: Allow D input**
- D == 1 (S input == 1): force output to 1
- D == 0 (R input == 1): force output to 0
- ~~S and R inputs == 0: preserve output~~
  - Output preserved if C == 0
- ~~S and R inputs == 1:~~
  - Invalid entry



Gated D Latch







Latch Feedback Issue

- Input:
  - A==0: No change
  - A==1: Invert state
- A==1 and C==1:
  - Instantaneous oscillation of Q without gap/stop