Processor Pipelining

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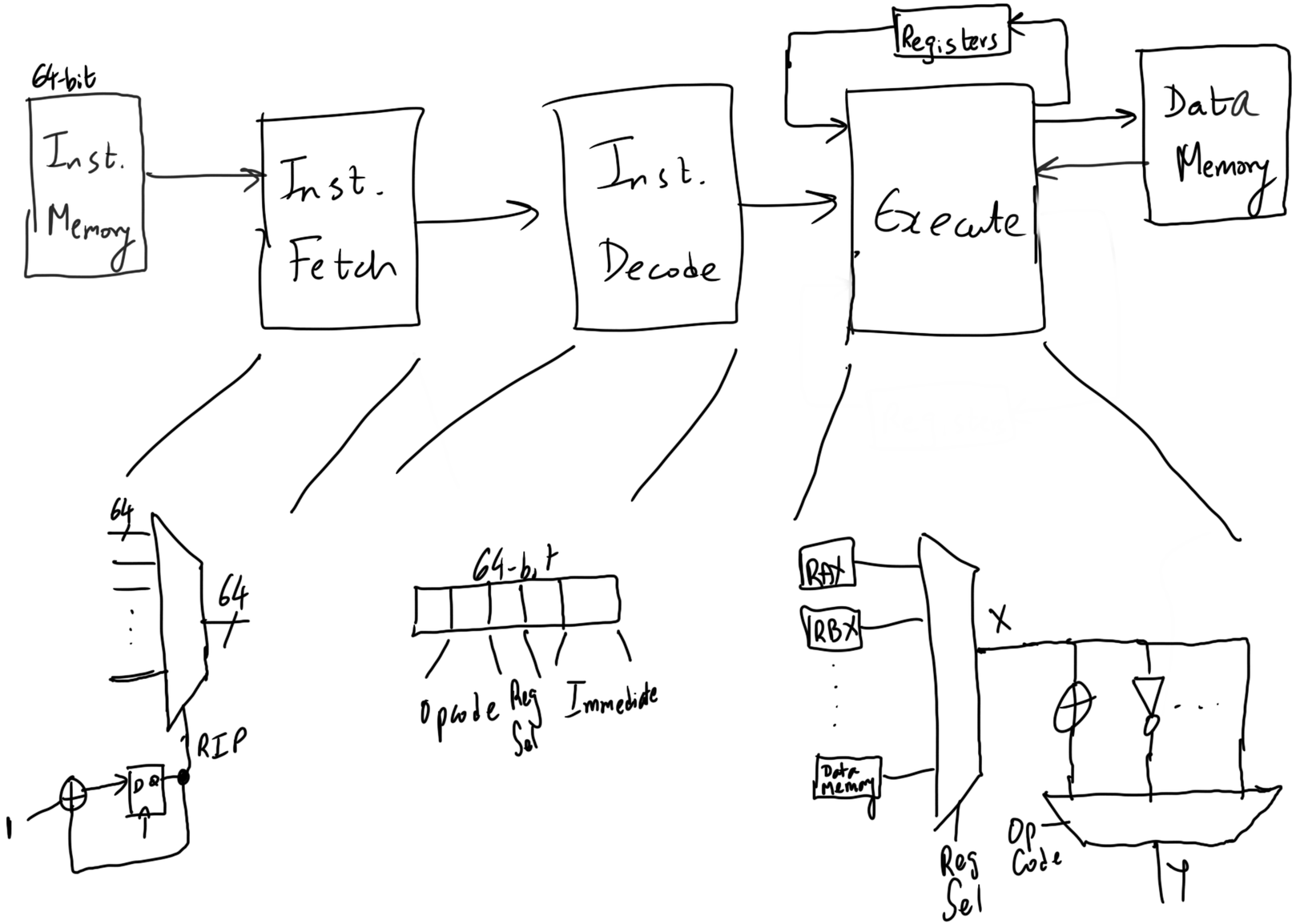
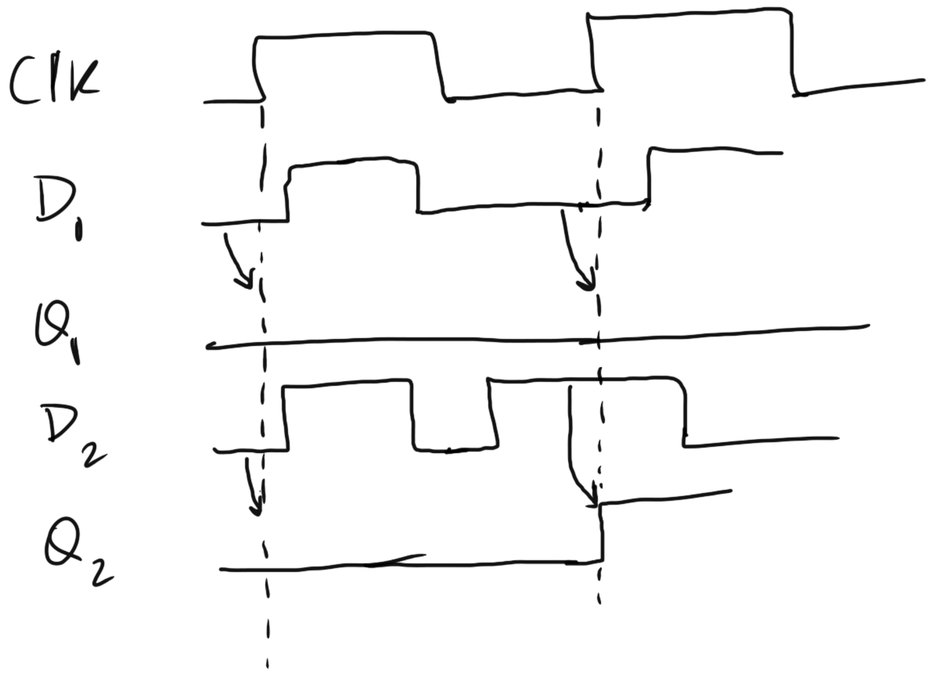
April 10, 2024

Processor Overview



Register input requirements

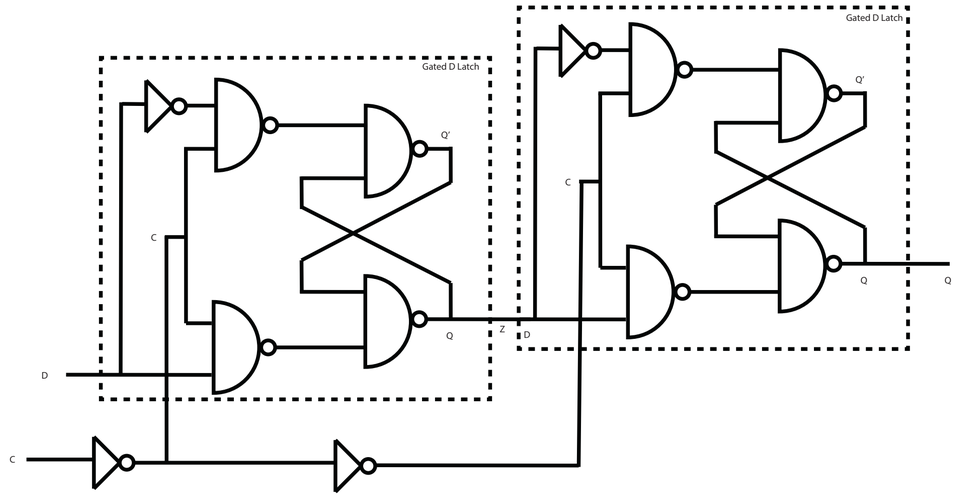
- D register
  - D input latched just before clk rising edge

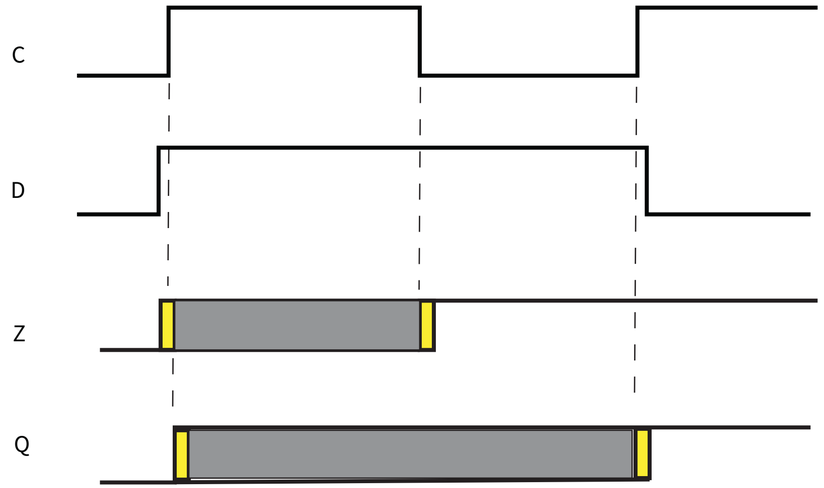


Positive-Edge Master-Slave D Flip-Flop

Setup Time

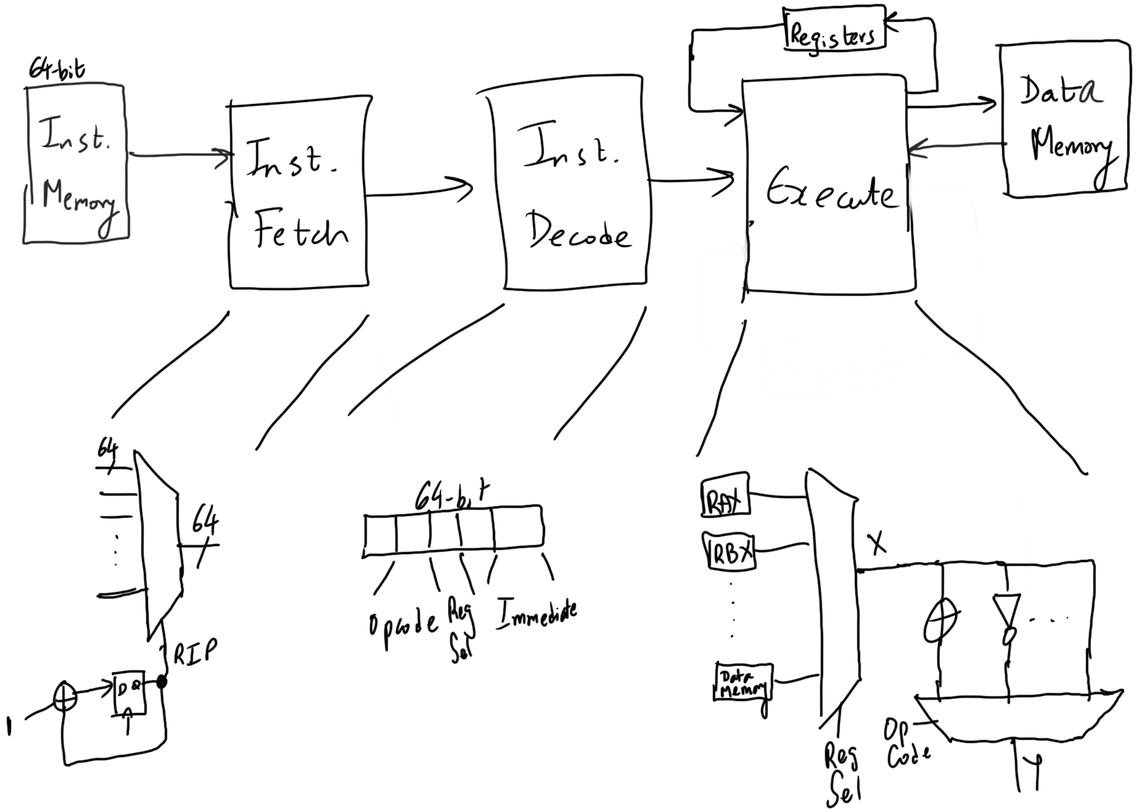
- D input need to be stable before C rising edge
- Race condition between D and C
- Avoid uncertainty of output

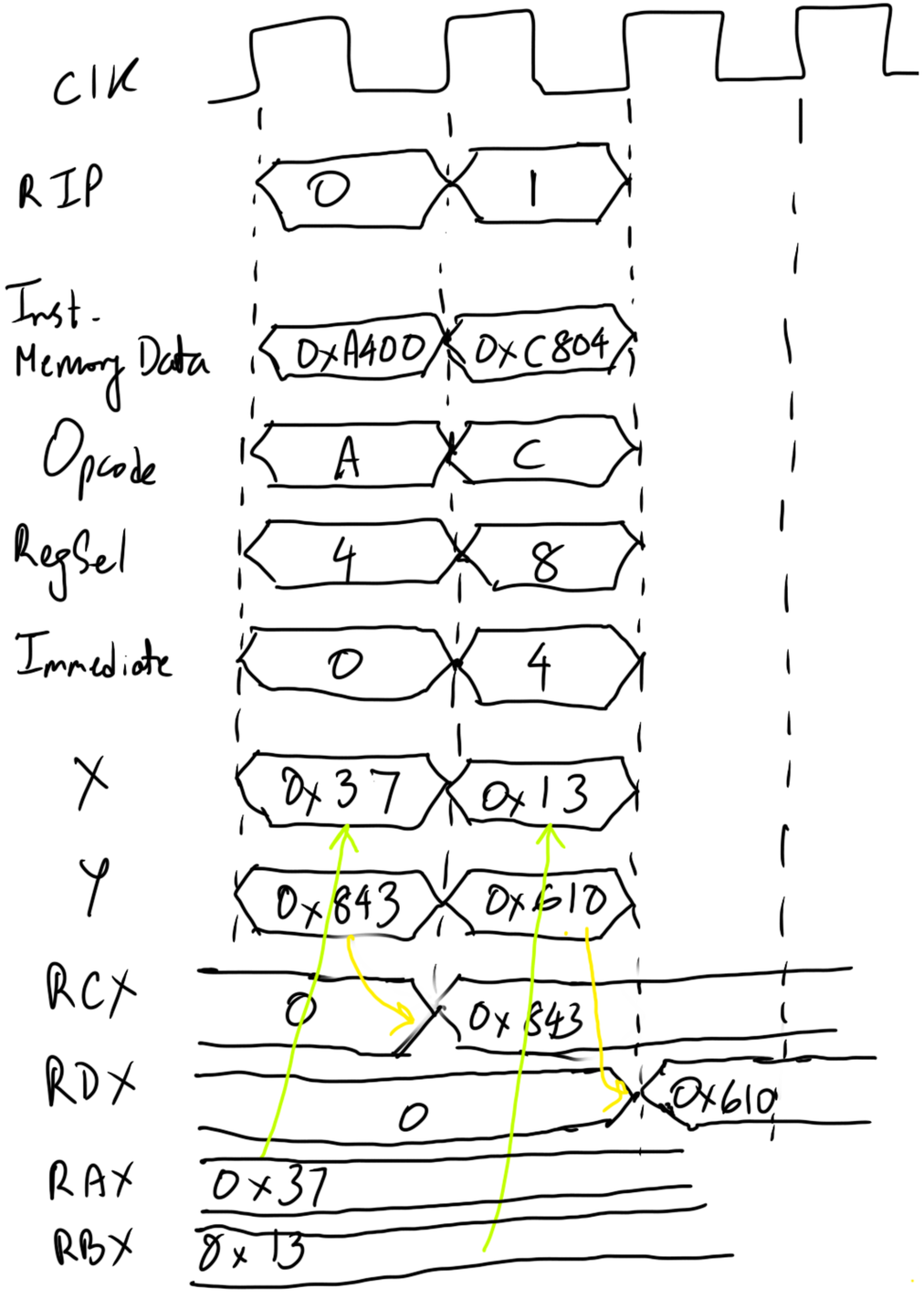




Setup Time

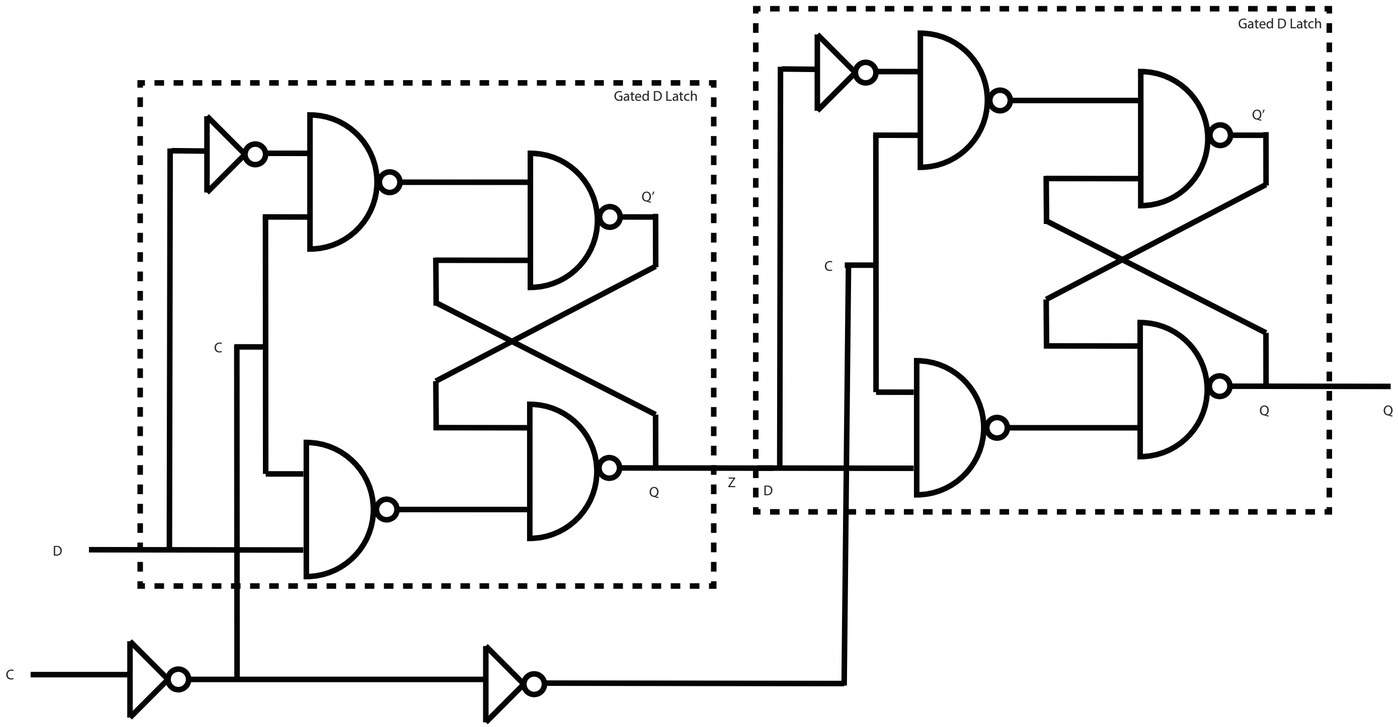
Signals example

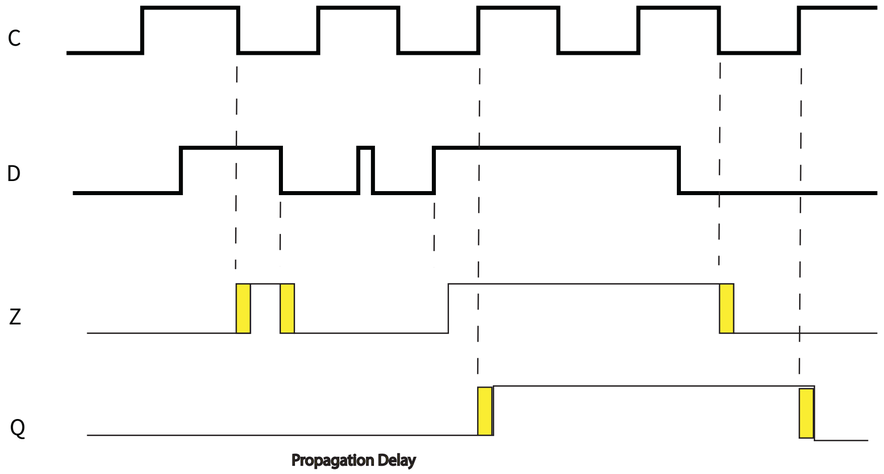




Positive-Edge Master-Slave D Flip-Flop

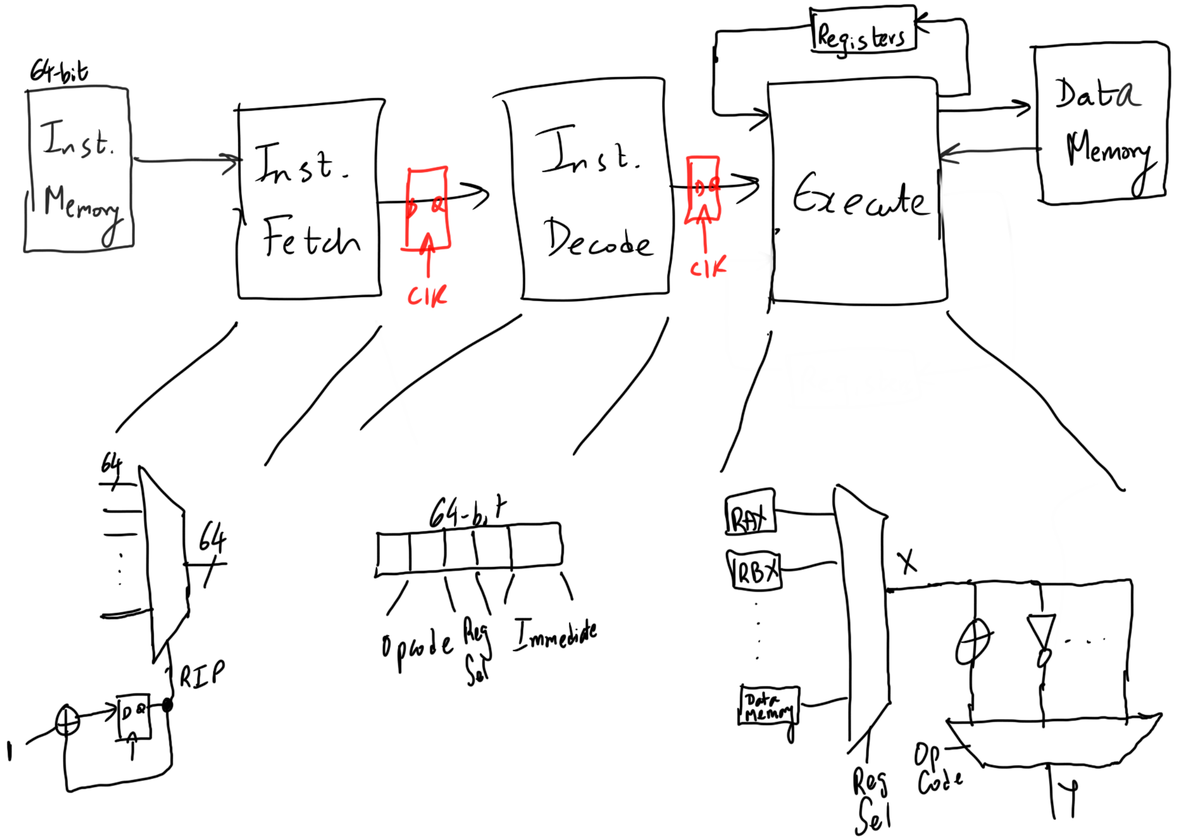
Timing Diagram with Propagation Delay





Pipelining

- Need to add registers in data path to reduce propagation delay in each clock cycle



Clock Frequency of Processor

- Trade-off between more complex operation performed in a clock cycle vs. faster clock frequency
- Example of a complex operation vs simple operation
  - Stages all combined together
  - Addition of 64 bits vs. Addition of 16 bits

Hazards/Dependency

- Read After Write
- Conditional Jump
- Especially true with more pipeline stages (x86 64 versions have more than 12)
  - Needed to run the clock at faster frequency