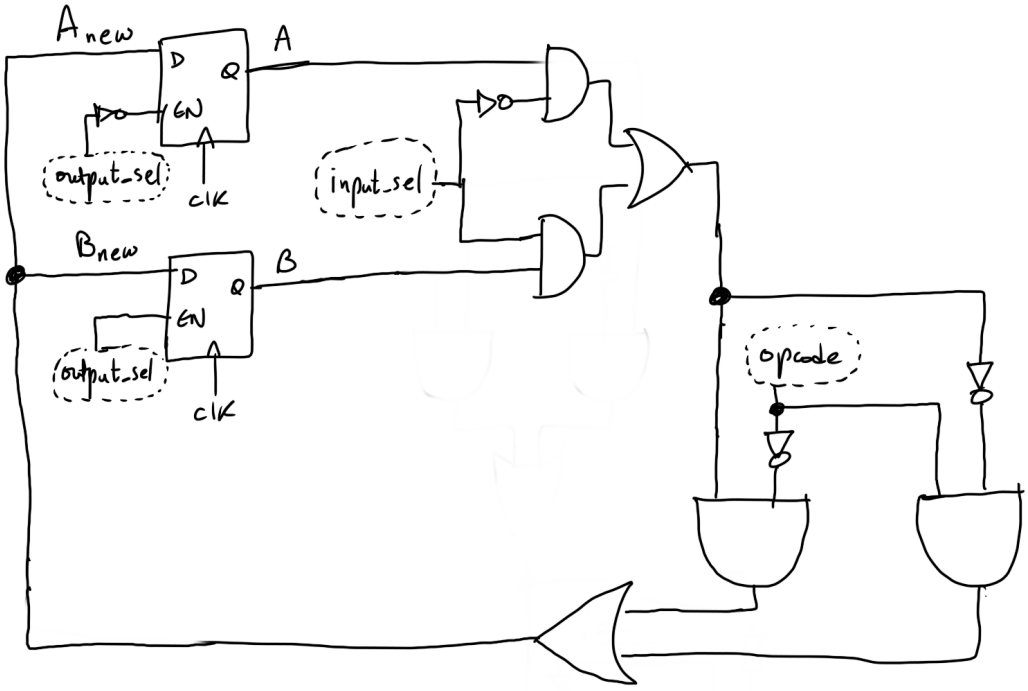
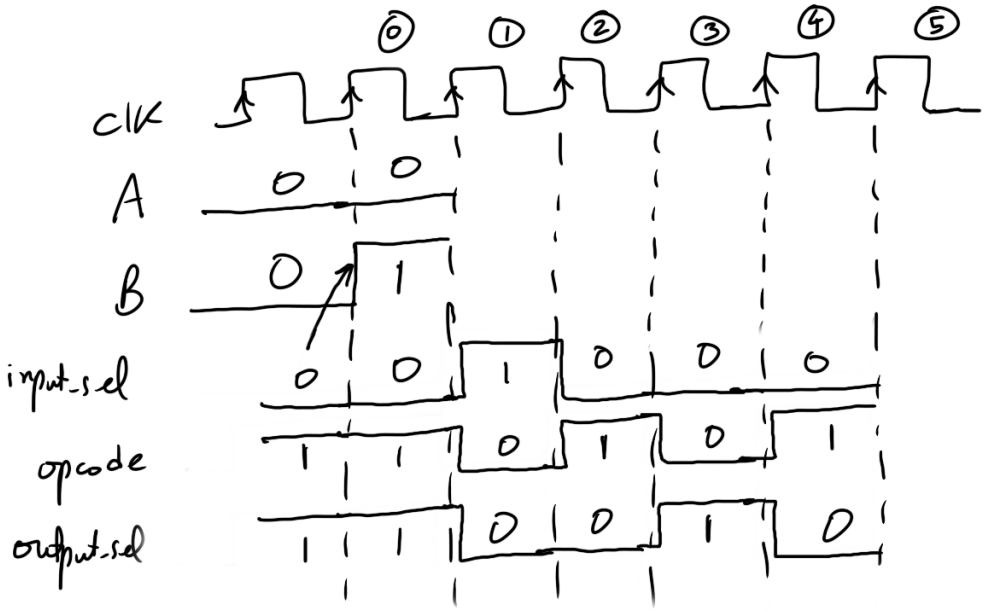
CMSC313 Mid-term Exam **Name:**

Closed book/notes. No electronics. (3 pages)
A lot of hints are provided below, no additional hints will be provided. If you have to make any additional assumptions, please list them out and continue solving the problem, showing work.

1. 25 points
Complete the timing diagram for the following circuit. Fill in the values for registers A and B for clock cycles 1 to 5. Label values as 0 or 1 for both A and B for each of the 5 clock cycles. The values for A and B would be dependent on control parameters labelled as input_sel, opcode and output_sel as shown in the block diagram below.
Hint: For values of A and B for cycle 1, find A_{new} and B_{new} values in cycle 0. Remember that A gets the value of A_{new} at the rising edge of clock going from cycle 0 to cycle 1.





2. Create a Finite State Machine to handle the following requirements. The output Z should be set when an ALU (comparison) instruction returns that the comparison was equal. If the instruction executed is not an ALU (comparison) instruction, the Z output should be left unchanged. There are two inputs in the system: A is 1 if the current instruction is an ALU (comparison) instruction, it is 0 otherwise. C is 1 if the ALU (comparison) instruction returned that the comparison was equal, it is 0 otherwise. Note that value of C should be ignored for non-ALU instructions, i.e., C should be ignored when A==0. The design can use either Mealy or Moore state machine. Assume that the registers for state bit(s) have EN==1 (D input is always forwarded to Q at the next clock rising edge) and the default/reset value for state bit(s) is/are 0. Assume that there will always be instructions executed every cycle, so no need to consider a freeze or stop condition.
Hint: Start with the default/reset state called NotEqual and assume that at reset, no ALU (comparison) instruction has run yet and Z will start at 0.

a. Transition Diagram (20 points). Hint: Show transition of all combinations of inputs for each state (AC=00,01,10,11).
b. Assign binary values to each state (5 points). Hint: If there are 1~2 states in the transition diagram, 1 bit of state is needed. If there are 3~4 states, 2 bits of state are needed, etc.
c. Truth Table (20 points)
d. Equations (for new value of state bit(s) and output) (20 points). Use any approach to show simplified equations. Show all work.
e. Block diagram, showing registers for each of the state bit(s) and combinational logic for the D inputs of the state bit(s) and the combinational logic for Z output. (10 points)

Bonus (10 points):
Write out the list of instructions performed by Problem 1 in clock cycles 1~5.
Hint: Cycle 0 instruction is based on the values of input_sel, opcode and output_sel in cycle -1 (i.e., the clock cycle before cycle 0). The instruction for clock cycle 0 is B = A'.

Cycle 1:

Cycle 2:

Cycle 3:

Cycle 4:

Cycle 5: