CMSC 313 HW1
Due 2/28/2024 11:59pm

Please submit the completed homework through Blackboard.

1. Design a 3-bit decrementing counter. The counter registers will start at 000 and in the next clock rising edge, it will have a value of 111. After 111, the counter will have a value of 110 at the next clock rising edge. Each register will have D input, R input, EN input and CLK input. Each register will have a Q output. Assume that a reset signal is provided that you connect to the R input of the register and not needed anywhere else. Show the block diagram with 3 registers and the combinational logic needed to drive the D and EN inputs of the 3 registers. The EN input can be fixed to 1 (D input is passed on to Q output every clock rising edge) or it can be driven by combinational logic. Show all work.
2. Design a Finite State Machine for a system where we want to allow a person into an amusement park only once. Imagine there is an app in the person's phone and it receives an input A that is 1 if the person is inside the park and 0 if the person is not inside the park. Hint: Let there be one state called Init and if the input A is 1, the FSM should go to InsidePark state. As with problem 1, design the combinational logic input to the D and En inputs of the registers (keeping track of the state). You can use any of the approaches discussed in class. Show all work.