CMSC313 Final Exam **Name:**

No electronic gadgets allowed. Closed book/notes. No copying allowed. Violations may result in 0 grade for the final.

There are 4 problems in this exam (5 pages total).

1.

Build a FSM that keeps track of whether a light bulb is currently on or off. There are two buttons (inputs) that manipulate the light bulb. Input I is used to flip the light bulb status. If the light bulb is already on, and if I is 1, the light bulb is then turned off. If the light bulb is off, and if I is 1, the light bulb is turned on. If I is 0, the light bulb isn't changed. The second input C is used to reset the fuse. If C is 1, the light bulb is forced to be turned off. If C is 0, the light bulb is not changed. If C is 1 and I is 1, C takes precedence and so the light bulb is forced off. When C is 1, the light bulb remains in off state. When C becomes 0 after that, the light bulb resumes normal operation through the I input. The output of the FSM Z is 1 if the light bulb is on, Z is 0 if the light bulb is off. Assume that at reset, the light bulb is off. You can use either Mealy or Moore design (i.e., it is fine if the output Z changes at the next clock rising edge instead of immediately after an input change).

a. Transition Diagram
b. State Assignment: Assign binary values for each state
c. Truth Table
d. K-Map
e. Equation for new value of state bit(s) and output
f. Block Diagram showing (a) register(s) for the state bit(s), (b) the combinational logic used to generate the D input (i.e., new value of state) of the register(s) and (c) the logic to generate the Z output from the state bits and/or inputs.

Use this page to show any additional work for problem 1.

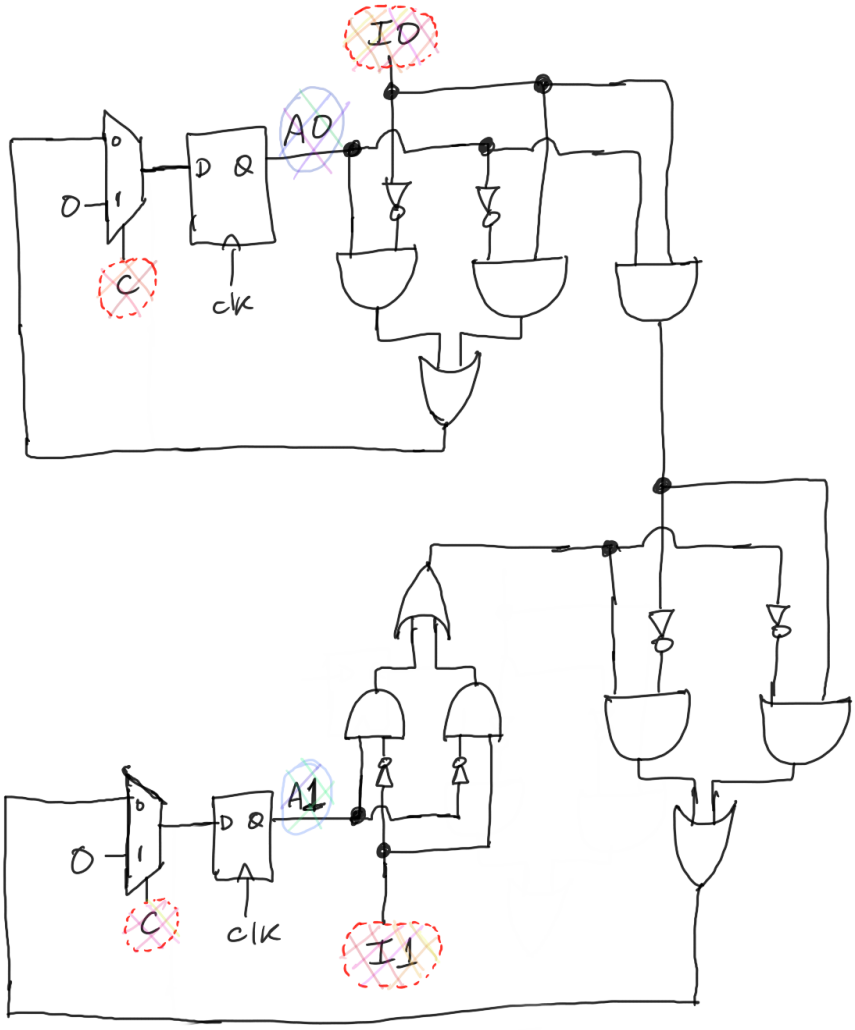
2.
Create the truth table for a 2-bit unsigned adder circuit. No need to go beyond just the truth table.
The adder performs addition of stored 2-bit (accumulator) value with input 2-bit (immediate) value.
The states of the adder are the following:
- Accumulator Bit 1 (A1)
- Accumulator Bit 0 (A0)

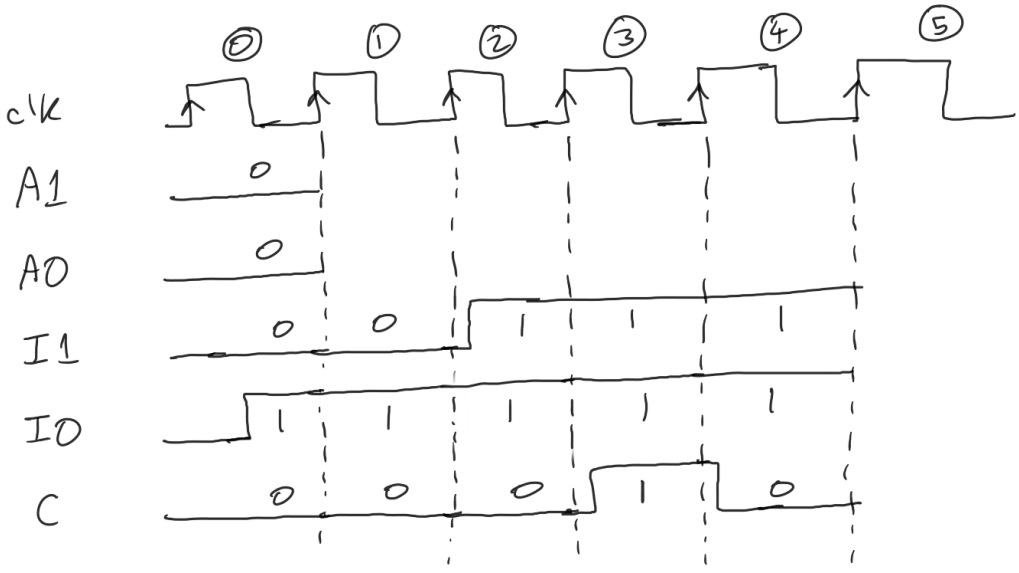
The inputs of the adder are the following:
- Immediate Value Bit 1 (I1)
- Immediate Value Bit 0 (I0)
- Clear (C): When C is 1, the A1 and A0 values are cleared to 0. When C is 0, the adder operation is performed.

The output of the adder is the following:
- Overflow (O)

The truth table should contain 32 rows with 5 input bits (A1old,A0old,I1,I0,C). There are 3 output bits (A1new,A0new,O).
Some examples:
- Let C=0. If Accumulator is 2, A1old=1 and A0old=0. If immediate value is 3, I1=1 and I0=1. The sum is $2+3=5_{10}=101_2$. So O=1,A1new=0,A0new=1.
- Let C=0. If Accumulator is 1, A1old=0 and A0old=1. If immediate value is 1, I1=0 and I0=1. The sum is $1+1=2_{10}=010_2$. So O=0,A1new=1,A0new=0.
- If C=1, A1old, A0old, I1,I0 values are not needed. If C=1, A1new=0 and A0new=0.

3.
For the following circuit and the input values in timing diagram, fill-in the timing diagram for the A1 and A0 states. Enter values for cycles 1-5. Hint: Find the D input of the registers first and then update Q output of the registers to be equal to D input at the next clock rising edge.





4.

a. How are problems 1 and 2 related? Briefly describe any relationship you observe.

b. Write out the equations for A0new and A1new (D inputs of the registers) in problem 3.

c. Based on 4b and the timing diagram in problem 3, briefly describe the functionality of the circuit in problem 3. Hint: see how A0new and A1new outputs are related to A0old, A1old, I1, I0 and C inputs. If it helps, write out a couple of rows in truth table (pick values for inputs and calculate the corresponding outputs).

c. Let us say that you want to build a processor to perform the operations in problem 3. What are the instructions you need to perform the operations, i.e., what are the different operations that need to be supported? The format of the instruction is not important, only the description of the operation is important.

d. Following on problem 4c, what are the fields needed in instruction memory to support the instructions and each of their bit-widths?

e. Following on problem 4c, write out the list of instructions performed in clock cycles 1-5. Hint: Cycle 1's instruction produces the state/output A1 and A0 that is observed in Cycle 1. A1 and A0 are based on the inputs in cycle 0 (i.e., inputs just before rising clock edge of cycle 1).

Cycle 1:

Cycle 2:

Cycle 3:

Cycle 4:

Cycle 5: